

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> ( Not for submission under 37 CFR 1.99)	Application Number		10001477
	Filing Date		2001-11-01
	First Named Inventor	Steve Roe	
	Art Unit	2123	
	Examiner Name	Jason Scott Proctor	
	Attorney Docket Number	CD01203M	

## U.S. PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code <sup>1</sup>	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	7042301	B1	2006-05-09	Sutardja, Sehat	Entire Document
	2	5594388	B1	1997-01-14	O'Shaughnessy et al.	Entire Document
	3	5963105	B1	1999-10-05	Nguyen	Entire Document
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9	7129793	B1	2006-10-31	Gramegna	Entire Document
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43	6026134	B1	2000-02-15	Duffy et al.	Entire Document
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**FOREIGN PATENT DOCUMENTS**

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	1	Application Number 11/850,260 (CD2007006): "Circuit and Method for Improving the Accuracy of a Crystal-less Oscillator Having Dual-Frequency Modes;" Wright et al.; 33 pages	<input type="checkbox"/>
	2	USPTO Non-Final Rejection for Application Number 11/850,260 (CD2007006) dated 03/06/2009; 7 pages	<input type="checkbox"/>
	3	USPTO Non-Final Rejection for Application Number 11/644,100 (CD05204) dated 03/09/2009; 11 pages	<input type="checkbox"/>
	4	USPTO Advisory Action for Application Number 11/644,100 (CD05204) dated 02/09/2009; 3 pages	<input type="checkbox"/>
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6	USPTO Non-Final Rejection for Application Number 11/644,100 (CD05204) dated 04/14/2008; 10 pages	<input type="checkbox"/>
7	USPTO Notice of Allowance for Application Number 11/415,588 (CD05028) dated 03/11/2008; 6 pages	<input type="checkbox"/>
8	USPTO Advisory Action for Application Number 11/415,588 (CD05028) dated 01/14/2008; 3 pages	<input type="checkbox"/>
9	USPTO Final Rejection for Application Number 11/415,588 (CD05028) dated 10/19/2007; 8 pages	<input type="checkbox"/>
10	USPTO Non-Final Rejection for Application Number 11/415,588 (CD05028) dated 06/13/2007; 8 pages	<input type="checkbox"/>
11	USPTO Notice of Allowance for Application Number 12/218,404 (CD05028C1) dated 03/19/2009; 7 pages	<input type="checkbox"/>
12	USPTO Non-Final Rejection for Application Number 12/218,404 (CD05028C1) dated 09/30/2008; 8 pages	<input type="checkbox"/>
13	Application Number 11/644,100 (CD05204): "Differential-to-single ended signal converter circuit and method," Stiff; 33 pages	<input type="checkbox"/>
14	Application Number 11/415,588 (CD05028): "Voltage Controlled Oscillator Delay Cell and Method," Sivadasan; 24 pages	<input type="checkbox"/>
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18	Application Number 11/132,894 (CD04064): "Open Loop Bandwidth Test Architecture and Method for Phase Locked Loop (PLL)," Stiff; 38 pages	<input type="checkbox"/>
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22	USPTO Advisory Action for Application Number 11/322,044 (CD05198) dated 11/30/2007; 2 pages	<input type="checkbox"/>
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25	Application Number 11/322,044 (CD05198): "Split charge pump PLL architecture," Stiff; 19 pages	<input type="checkbox"/>
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30	Application Number 09/849,164 (CD01035): "Reduced Static Phase Error CMOS PLL Charge Pump," Stiff; 30 pages	<input type="checkbox"/>
31	Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques," IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996; 10 pages	<input type="checkbox"/>
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37	USPTO Notice of Allowance for Application Number 10/871,582 (CD03036) dated 03/30/2006; 6 pages	<input type="checkbox"/>
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39	USPTO Non-Final Rejection for Application Number 10/871,582 (CD03036) dated 09/07/2005; 7 pages	<input type="checkbox"/>
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42	USPTO Final Rejection for Application Number 09/404,891 (CD99054) dated 12/08/2004; 7 pages	<input type="checkbox"/>
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## **U.S. PATENT APPLICATION PUBLICATIONS**

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	1	Application Number 10/226,911 (CD02112): "Calibration of Integrated Circuit Time Constants," Gehring et al.; 32 pages	<input type="checkbox"/>
	2	USPTO Notice of Allowance for Application Number 09/943,149 (CD01085) dated 01/12/2004; 7 pages	<input type="checkbox"/>
	3	USPTO Non-Final Rejection for Application Number 09/943,149 (CD01085) dated 08/28/2003; 9 pages	<input type="checkbox"/>
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6	Application Number 09/943,149 (CD01085): "Method for Phase Locking in a Phase Lock Loop," Moyal et al.; 21 pages	<input type="checkbox"/>
7	Durham et al., "Integrated Continuous-Time Balanced Filters for 16-bit DSP Interfaces," IEEE, 1993; 6 pages	<input type="checkbox"/>
8	Durham et al., "Circuit Architectures for High Linearity Monolithic Continuous-Time Filtering," IEEE, 1992; 7 pages	<input type="checkbox"/>
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Application Number	10001477
Filing Date	2001-11-01
First Named Inventor	Sieve Roe
Art Unit	2123
Examiner Name	Jason Scott Proctor
Attorney Docket Number	CD01203M

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	1	USPTO Advisory Action for Application Number 11/200,619 (CD04112) dated 05/11/2009; 3 pages	<input type="checkbox"/>
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6	USPTO Non-Final Rejection for Application Number 11/201,922 (CD04111) dated 10/21/2008; 12 pages	<input type="checkbox"/>
7	USPTO Final Rejection for Application Number 11/201,922 (CD04111) dated 04/30/2008; 10 pages	<input type="checkbox"/>
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Application Number	10001477
Filing Date	2001-11-01
First Named Inventor	Steve Roe
Art Unit	2123
Examiner Name	Jason Scott Proctor
Attorney Docket Number	CD01203M

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35	6049223	B1	2000-04-11	Lytle et al.	Entire Document
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# **INFORMATION DISCLOSURE STATEMENT BY APPLICANT**

( Not for submission under 37 CFR 1.99)

Application Number		10001477
Filing Date		2001-11-01
First Named Inventor	Steve Roe	
Art Unit	2123	
Examiner Name	Jason Scott Proctor	
Attorney Docket Number	CD01203M	

42	6130552	B1	2000-10-10	Jefferson et al.	Entire Document
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44	6049225	B1	2000-04-11	Huang et al.	Entire Document
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	1	20080186052	A1	2008-08-07	Needham et al.	Entire Document
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	1	Kory Hopkins, "Definition;" 01/16/1997; <http://www.cs.sfu.ca/cs/people/GradStudent.html>; 1 page	<input type="checkbox"/>
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9	USPTO Notice of Allowance for Application Number 09/475,879 (CD99047) dated 10/22/2004; 7 pages	<input type="checkbox"/>
10	USPTO Advisory Action for Application Number 09/475,879 (CD99047) dated 03/04/2002; 3 pages	<input type="checkbox"/>
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12	USPTO Final Rejection for Application Number 09/475,879 (CD99047) dated 10/11/2001; 10 pages	<input type="checkbox"/>
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19	USPTO Non-Final Rejection for Application Number 10/137,497 (CD01197M) dated 11/05/2004; 17 pages	<input type="checkbox"/>
20	USPTO Final Rejection for Application Number 10/137,497 (CD01197M) dated 05/05/2005; 13 pages	<input type="checkbox"/>
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23	USPTO Non-Final Rejection for Application Number 10/137,497 (CD01197M) dated 08/02/2006; 21 pages	<input type="checkbox"/>
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25	USPTO Notice of Allowance for Application Number 10/137,497 (CD01197M) dated 07/20/2007; 4 pages	<input type="checkbox"/>
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Doc code: IDS

PTO/SB/08a (06-09)

Doc description: Information Disclosure Statement (IDS) Filed

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Examiner Initial*	Cite No	Publication Number	Kind Code*	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
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	1	Application Number 11/273,708 (CD05141): "Capacitance Sensor Using Relaxation Oscillators," Snyder et al.; 33 pages	<input type="checkbox"/>
	2	USPTO Non-Final Rejection for Application Number 11/273,708 (CD05141) dated 03/19/2007; 16 pages	<input type="checkbox"/>
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5	Application Number 11/337,272 (CD05191): "Successive Approximate Capacitance Measurement Circuit," Snyder; 29 pages	<input type="checkbox"/>
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8	USPTO Final Rejection for Application Number 11/337,272 (CD05191) dated 02/02/2007; 11 pages	<input type="checkbox"/>
9	USPTO Advisory Action for Application Number 11/337,272 (CD05191) dated 04/03/2007; 3 pages	<input type="checkbox"/>
10	USPTO Non-Final Rejection for Application Number 11/337,272 (CD05191) dated 05/17/2007; 11 pages	<input type="checkbox"/>
11	USPTO Notice of Allowance for Application Number 11/337,272 (CD05191) dated 08/15/2007; 9 pages	<input type="checkbox"/>
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15	USPTO Non-Final Rejection for Application Number 11/698,660 (CD05176) dated 12/02/2008; 12 pages	<input type="checkbox"/>
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17	Application Number 11/709,866 (CD05170): "Input/Output Multiplexer Bus," Dennis Sequine; 33 pages	<input type="checkbox"/>
18	USPTO Non-Final Rejection for Application Number 11/709,866 (CD05170) dated 11/07/2008; 14 pages	<input type="checkbox"/>
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21	Van Ess, David, "Simulating a 555 Timer with PSoC," Cypress Semiconductor Corporation, Application Note AN2286, May 19, 2005; 10 pages	<input type="checkbox"/>
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Doc description: Information Disclosure Statement (IDS) Filed

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